REMARKS

In accordance with the foregoing, claims 1, 3-19, 21-27, and 29-30 have been amended, claims 19, 23, 29, and 30 have been cancelled without prejudice or disclaimer, and claim 31 has been added. No new matter is being presented, and approval and entry are respectfully requested.

Claims 17 and 20-22 stand objected to, but would be allowable if rewritten in independent form incorporating the recitations of the base claims. Because claims 20-22 have been amended incorporating the recitations of claim 19, it is respectfully requested that claims 20-22 be allowed. Claims 24-28 stand in condition for allowance.

Claims 1-30 are pending and under consideration.

REJECTION UNDER 35 U.S.C. § 112:

In the Office Action, at page 2, claims 1-6 are rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness.

In response, the claims have been amended to improve clarity and antecedent support.

Accordingly, it is respectfully requested that the § 112, second paragraph rejections of the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 3, claims 1-5, 7, 8, 10, 11, 12, 14-16, and 30 are rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6,167,479 to Hartnett et al. ("Hartnett"). This rejection is traversed and reconsideration is requested.

Harnett generally provides a Jump Predict Subsection 151 and an Instruction Address Generation Subsection 152 provide absolute addresses to the Instruction Cache Tag Logic 153 as shown in FIG. 6 and corresponding description.

However, Harnett is silent as to teaching or suggesting "a specific application-purpose instruction operating unit supporting a flexible pipeline structure and carrying out an operation of the specific application-purpose operation instruction for each application field," as recited in independent claims 1 and 31. Although Harnett calls each unit 151 and 152 a subsection, that alone doe not teach or suggest that "an operation of the specific application-purpose operation instruction for each application field," is carried out as recited in independent claims 1 and 31.

The subsections 151 and 152 merely output absolute addresses to logic 153.

In addition, Harnett generally describes a system and method allowing execution to continue on an Nth instruction for a variable number of additional cycles 118. See column 7, lines 55-67. Further, an Instruction Read Address Control Logic 154 provides the address to the Instruction First-Level Cache (I-FLC) 14 on Address Path 156. The address is used to retrieve eight instructions from each of the eight memory blocks (not shown) of the I-FLC 14. See column 8, lines 26-44.

However, Harnett is silent as to teaching or suggesting, "a rewritable register prescribing a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue the same instructions, wherein the instruction of said specific application-purpose instruction occupies an operating unit source," as recited in independent claim 1. The cited reference does not broach the concept of providing the recitations of the rewritable register recited in independent claim 1.

Referring to independent claim 7, according to Harnett, once recovery actions are accomplished, execution may be re-started with the instruction stream being executed at the time the interrupt occurred. See column 12, lines 5-51. Further, a microcode controller assumes control of control lines 176. The controller provides control signals to the memory interface 160 and to the other logic sections. However, Harnett fails to teach or suggest, "an exception processing unit carrying out the exceptional processing when the operation exception is detected during the execution of the specific application-purpose operation instruction," as recited in independent claim 7. Even assuming, *arguendo*, that Harnett provides determining what caused an interrupt, the cited reference does not provide that the determination is done "during the execution of the specific application-purpose operation instruction," as recited in independent claim 7. Similar arguments apply to support the patentability of independent claim 11.

In view of the foregoing, it is respectfully requested that the pending claims be allowed.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 7, claims 9, 13, and 18 are rejected under 35 U.S.C. § 103 in view of Hartnett and U.S. Patent No. 6,553,513 to Swoboda et al. ("Swoboda"). The rejection is traversed and reconsideration is requested.

The arguments presented above are incorporated herein to support the patentability of claims 9/7, 13/11, and 18/11 over Hartnett.

Referring to Swoboda, this reference generally describes emulation and debugs circuitry that can be incorporated into a variety of digital systems. See abstract. Interrupts are classified and processed accordingly when the processor is stopped by a debug event. The cited reference also provides a break on a software breakpoint instruction (instruction replacement) and a break on a specified program or data access without requiring instruction replacement (accomplished using bus comparators). See column 8, lines 20-23.

However, similarly to Harnett, Swoboda is silent as to teaching or suggesting, "an exception processing unit carrying out the exceptional processing when the operation exception is detected during the execution of the specific application-purpose operation instruction," as recited in independent claim 7. The cited reference does not provide that the determination is done "during the execution of the specific application-purpose operation instruction," as recited in independent claim 7. Similar arguments apply to support the patentability of independent claim 11.

In view of the foregoing, it is respectfully requested that the pending claims be allowed.

In the Office Action, at page 8, claims 19, 23, and 29 are rejected under 35 U.S.C. § 103 in view of Hartnett and U.S. Patent No. 6,553,513 to Swoboda et al. ("Swoboda"). The rejection is traversed and reconsideration is requested.

Referring to claims 19, 23, and 29, because these claims have been cancelled without prejudice or disclaimer, it is respectfully asserted that the rejection to the claims is hereby rendered moot.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner's contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: August 16, 2004

By: _____
Alicia M. Choi
Registration No. 46,621

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

CERTIFICATE UNDER 37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Trademarks, 2900 Crystal Drive, Arlington, VA 22202-3513
on August 16, 2004
STAAS & HALSEY
By: _____
Date August 16, 2004